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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/433,705

Applicant(s)

YAMAZAKI, SHUNPEI

Examiner

Steven Loke

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-17 and 46-82 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-17, 47, 48, 51-69, 71-75 and 77-82 is/are rejected.
- 7) ☒ Claim(s) 46, 49, 50, 70 and 76 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date: 3/2/04
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

1. Since the applicant will file a request to enter the amendment filed on 1/14/04, the present Official Action will be based on the amendment filed on 1/14/04.

2. The disclosure is objected to because of the following informalities:

It is believed that regions 316 to 319, 326 and 327 are undoped regions in fig. 12A. It is unclear why regions 316 to 319, 326 and 327 are n^- - type impurity regions (page 26, lines 21-22). The reference numerals should refer to the shaded regions instead of the unshaded regions.

It is believed that regions 334 and 335 are undoped regions in fig. 12B. It is unclear why regions 334 and 335 are n^- - type impurity regions (page 27, line 7). The reference numerals should refer to the shaded regions instead of the unshaded regions.

Appropriate correction is required.

3. Claim 46-50, 70 and 76 are objected to because of the following informalities: Claim 46, line 11, the phrase "said second n-channel thin film transistor" has no antecedent basis. Appropriate correction is required.

4. Claim 47 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 12B discloses the vertical side edges of the lower portion of the gate wiring [370] of the p-channel TFT are coextensive with the vertical side edges of the upper portion of the gate wiring [370] of the p-channel TFT. The specification never discloses top

surfaces of the tapered portions of the third conductive layers and a top surface of the gate insulating film is in a range of 3 to 60 degrees as claimed in claim 47.

5. Claim 48 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 48, lines 1-2, the phrase "the semiconductor island" is unclear whether it is being referred to the first semiconductor island or the second semiconductor island of claim 46.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 13, 15-17, 51, 53-55, 57-60, 62-64, 66-69, 71-74, 81 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. (Japanese patent application no. 06-148685) in view of Kurokawa.

In regards to claims 13, 51, 69 and 71, Nakazono et al. disclose a semiconductor device in figs. 1-3. It is a liquid crystal display device, comprising: at least one first thin film transistor (TFT) (the TFT on left side of fig. 2) formed over an insulating substrate [1]; a pixel electrode [11] electrically connected to the first thin film transistor; a driver circuit including at least one second thin film transistor (the TFT on right side of fig. 2) formed over the substrate [1] for driving the at least one first thin film transistor, each of the first and second thin film transistors comprising: a semiconductor island [2] on an

insulating surface [1]; source and drain regions [7a] formed in the semiconductor island; a channel region [7c] in the semiconductor island between the source and drain regions [7a]; a pair of lightly doped regions [7b] formed between the channel region [7c] and the source and drain regions [7a] wherein an impurity concentration in the lightly doped regions [7b] is smaller than that in the source and drain regions [7a]; a gate electrode [4, 5] formed over the semiconductor island with a gate insulating film [3] interposed therebetween wherein said gate electrode [4, 5] comprises at least a first conductive layer [4] and a second conductive layer [5] formed on the first conductive layer [4].

Nakazono et al. differs from the claimed invention by not showing each of the first and second thin film transistors comprises the first conductive layer having a pair of tapered portions, which extend beyond side edges of the second conductive layer. In addition, the pair of lightly doped regions has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer, and a pair of second portions, which extend beyond side edges of the first conductive layer, and wherein the impurity concentration in the pair of first portions is smaller than the impurity concentration in the pair of second portions.

Kurokawa shows a semiconductor device comprising a gate electrode [33] having a first conductive layer [31] having a pair of tapered portions, which extend beyond side edges of the second conductive layer [32] in fig. 2. In addition, a pair of lightly doped regions [25] has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer [31], and a pair of second portions, which extend beyond side edges of the first conductive layer [31]. Since the pair of lightly doped

regions [25] are formed by ion-implantation and then by diffusion, the impurity concentration at the bottom portion of each of the first portions of regions [25] would be smaller than the impurity concentration at the middle portion of each of the second portions of regions [25].

Since both Nakazono et al. and Kurokawa teach an insulated gate electrode having two conductive layers and a pair of lightly doped regions, it would have been obvious to have the gate electrode structure and the lightly doped regions of Kurokawa in each of the thin film transistors of Nakazono et al. because they prolong the life of the transistor and restrain the short channel effect.

It is inherent that the semiconductor device is an active matrix display device because it comprises a TFT array.

In regards to claims 55, 60, 64, 72-74, Nakazono et al. disclose a semiconductor device in figs. 1-3. It is a liquid crystal display device, comprising: at least one first thin film transistor (TFT) (the TFT on left side of fig. 2) formed over an insulating substrate [1]; a pixel electrode [11] electrically connected to the first thin film transistor; a driver circuit including at least one second thin film transistor (the TFT on right side of fig. 2) formed over the substrate [1] for driving the at least one first thin film transistor, each of the first and second thin film transistors comprising: a semiconductor island [2] on an insulating surface [1]; source and drain regions [7a] formed in the semiconductor island; a channel region [7c] in the semiconductor island between the source and drain regions [7a]; a pair of lightly doped regions [7b] formed between the channel region [7c] and the source and drain regions [7a] wherein an impurity concentration in the lightly doped

regions [7b] is smaller than that in the source and drain regions [7a]; a gate electrode [4, 5] formed over the semiconductor island with a gate insulating film [3] interposed therebetween wherein said gate electrode [4, 5] comprises at least a first conductive layer [4] and a second conductive layer [5] formed on the first conductive layer [4].

Nakazono et al. differs from the claimed invention by not showing each of the first and second thin film transistors comprises the first conductive layer having a pair of tapered portions, which extend beyond side edges of the second conductive layer. In addition, the pair of lightly doped regions has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer, and a pair of second portions, which extend beyond side edges of the first conductive layer, and the concentration of the impurity in the pair of first portions monotonically increases in a direction from the channel region toward the source and drain regions.

Kurokawa shows a semiconductor device comprising a gate electrode [33] having a first conductive layer [31] having a pair of tapered portions, which extend beyond side edges of the second conductive layer [32] in fig. 2. In addition, a pair of lightly doped regions [25] has a pair of first portions, which are overlapped by the pair of the tapered portions of the first conductive layer [31], and a pair of second portions, which extend beyond side edges of the first conductive layer [31]. Since the pair of lightly doped regions [25] are formed by ion-implantation and then by diffusion, the impurity concentration at the bottom portion of each of the first portions of regions [25] would be smaller than the impurity concentration at the middle portion of each of the second portions of regions [25] in a direction from the channel region toward the source and

drain regions. Therefore, it is inherent that the impurity concentration at the bottom portion of each of the first portions of regions [25] monotonically increases toward the middle portion of each of the second portions of regions [25] in a direction from the channel region toward the source and drain regions.

Since both Nakazono et al. and Kurokawa teach an insulated gate electrode having two conductive layers and a pair of lightly doped regions, it would have been obvious to have the gate electrode structure and the lightly doped regions of Kurokawa in each of the thin film transistors of Nakazono et al. because they prolong the life of the transistor and restrain the short channel effect.

It is inherent that the semiconductor device is an active matrix display device because it comprises a TFT array.

In regards to claims 15, 53, 57, 66, 81, the combined device further discloses the semiconductor island comprises crystalline silicon.

In regards to claims 16, 54, 58, 62, 67, the combined device further discloses the first conductive layer includes an n-type silicon containing phosphorus and the second conductive layer includes tungsten silicide.

In regards to claims 17, 59, 63, 68, 82, the combined device of Nakazono et al. and Kurokawa further discloses the liquid crystal display can be used in a rear-type projector (a liquid crystal television) (page 5, lines 15-18 of the English translation of Nakazono et al.).

8. Claims 14, 52, 56, 61 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. in view of Kurokawa, further in view of Maddox, III.

In regards to claims 14, 52, 56, 61 and 65, Nakazono et al. and Kurokawa differ from the claimed invention by not showing an angle between the top surfaces of the tapered portions of the first conductive layer and a top surface of the gate insulating film is in a range of 3 to 60 degrees.

Maddox, III discloses an angle between top surfaces of the tapered portions of the gate electrode and a top surface of the gate insulating film is less than 60 degrees in fig. 2.

Since both Kurokawa and Maddox, III teach an insulated gate transistor having a tapered gate electrode, it would have been obvious to have the tapered gate electrode of Maddox, III in Kurokawa because it minimizes the problem of punchthrough in the thin film transistor.

9. Claims 75 and 77-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazono et al. in view of Kurokawa, further in view of Hamada.

In regards to claims 75 and 77-80, Nakazono et al. and Kurokawa differ from the claimed invention by not showing the active matrix display device is an electroluminescent display device.

Hamada discloses an active matrix display device is an electroluminescent display device [201] in fig. 8.

Since both Nakazono et al. and Hamada teach a display device includes a thin film transistor as a switching element, it would have been obvious to have the electroluminescent display element of Hamada to replace the liquid crystal element of Nakazono et al. because it provides a much clear image than liquid crystal.

10. Applicant's arguments filed 1/14/04 have been fully considered but they are not persuasive.

It is urged, in page 16 of the remarks, that the impurity could be doped in all the regions between the channel formation region and the n-type impurity regions which is not overlapped with the lower conductive layer of the gate electrode. However, neither the figures nor the specification shows the impurity could be doped in all the regions between the channel formation region and the n-type impurity regions which is not overlapped with the lower conductive layer of the gate electrode. Figs. 4A to 4D, 12A, and 12B only show the impurity could be doped in part of the regions between the channel formation region and the n-type impurity regions which is not overlapped with the lower conductive layer of the gate electrode. It is requested that the Applicant correct the figures so that the arrows of the above reference numerals are pointing to the low concentration impurity regions.

It is urged, in pages 18-19 of the remarks, that It is unclear how or why one of ordinary skill in the art would have been motivated to combine the device of Nakazono with Kurokawa, when the Kurokawa device includes SiO₂ films as masks. It is also urged that the second portions are formed by using SiO₂ [26] as masks. However, Kurokawa discloses the second portions of the LDD regions [25] are formed by slanting rotation ion implantation using the gate electrode as the mask. The silicon dioxide films [26] are used to formed the source and drain regions [27]. Since Nakazono also has highly doped regions [7a], it is proper to have the silicon dioxide films [26] of Kurokawa in Nakazono. Therefore, it is reasonable to combine Kurokawa and Nakazono.

It is urged, in page 19 of the remarks, that the Official Action has not given any indication that one with ordinary skill in the art at the time of the invention would have had a reasonable expectation of success when combining Nakazono and Kurokawa. However, the Official Action stated that the combined device of Nakazono and Kurokawa would prolong the life of the transistor and restrain the short channel effect. Therefore, there is a reasonable expectation of success when combining Nakazono and Kurokawa.

It is also urged, in page 19 of the remarks, that there is a lack of suggestion as to why a skilled artisan would use the proposed modifications to achieve the unobvious advantages first recognized by the Applicant. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. Since Kurokawa teaches the advantages of his structure in a LDD type MOSFET, it is reasonable to have his structure in other type of LDD type MOSFET. Therefore, it is desirable to combine the device of Kurokawa and Nakazono. The combined device would produce a device similar to the claimed invention. The combined devices of Nakazono, Kurokawa, Maddox and Hamada also disclose the claimed structures in the dependent claims.

11. Claim 46 would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl

March 3, 2004

Steven Loke
Primary Examiner

Handwritten signature of Steven Loke in cursive script.